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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,327	08/19/2003	Jean Khawand	CE11193JI210	4001
22917 7590 04/13/2007 MOTOROLA, INC. 1303 EAST ALGONQUIN ROAD IL01/3RD SCHAUMBURG, IL 60196			EXAMINER SORRELL, ERON J	
			ART UNIT	PAPER NUMBER
			2182	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	04/13/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

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Office Action Summary

Application No.

10/643,327

Applicant(s)

KHAWAND ET AL.

Examiner

Eron J. Sorrell

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 February 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 August 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/13/07 has been entered.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 7-11, 15, 18, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Johanson et al. (U.S. Patent No. 6,912,716 hereinafter "Johanson") in view Ellsworth et al. (U.S. Patent No. 6,131,113 hereinafter "Ellsworth").

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3. Referring to apparatus claim 1 and method claim 11,

Johanson teaches an electronic device, comprising:

a first processor (item 500, figure 4);

a second processor coupled to the first processor (item 502, figure 4);

shared memory coupled to the first and second processors, wherein the shared memory includes the transmit memories of both the first and second processors (see item 504 in figure 4); and

Johanson teaches the first processor is a master processor that manages the shared memory and allocates a message buffer to the second processor based on a specific request from the second processor to send a message to the first processor (see lines 31-43 of column 5 and lines 44-50 of column 6), note only the first processor allocates memory to the second processor when the second processor requests additional memory).

Johanson fails to teach the first processor sends a message buffer pointer to the second processor that directs the second processor to the message buffer.

Ellsworth teaches in an analogous system, a first processor allocating the shared memory (see lines 16-37 of column 3, note the shared resource disclosed by Ellsworth is shared memory (see

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lines 7-12 of column 5)). Ellsworth further teaches sending a message buffer pointer (see lines 23-39 of column 6) to the second processor that directs the second processor to the message buffer (see paragraph bridging columns 8 and 9, note the pointer is sent to the second processor via the resource queue).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Johanson with the above teachings of Ellsworth. One of ordinary skill would have been motivated in order to reduce the overhead associated with other methods of sharing memory between two processors as suggested by Ellsworth (see lines 51-67 of column 3).

4. Referring to claim 2, Johanson teaches the first processor responds to a reception of an empty buffer request from the second processor (see lines 31-43 of column 5), and Ellsworth teaches sending the message buffer pointer to the second processor (see paragraph bridging column 8 and 9).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the apparatus of Johanson with the above teachings of Ellsworth for the same reasons as mentioned in the rejection of claim 1, *supra*.

5. Referring to claim 3, Johanson teaches after receiving the message buffer pointer the second processor fills the message buffer with the message (see lines 51-57 of column 5).

6. Referring to claim 7, Johanson teaches a plurality of buffers assigned to the second processor are located in the shared memory (see item 44 in figure 1A).

7. Referring to claim 8, Johanson teaches the plurality of buffers assigned to the second processor are used by the second processor without having to request them from the first processor (see lines 18-27 of column 4).

8. Referring to claim 9, Johanson teaches that when the second processor needs to send a message to the first processor it loads a starting address of the message in one of the plurality of buffers assigned to the second processor (see lines 18-27 of column 4).

9. Referring to claim 10, Ellsworth teaches in an analogous system having first and second processor and a shared memory for

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use in telecommunications applications wherein the device is a radio device (see lines 25-33 of column 9).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the apparatus of Johanson with the above teachings of Ellsworth because Johanson suggests the device is used in telecommunication applications (see lines 62-67 of column 6).

10. Referring to claim 15, Johanson teaches a method for providing inter-processor communication between first and second processors using a shared memory that includes the transmit memories of the first and second processors, (see paragraphs bridging columns 2 and 3), the first processor being a master processor assigned to manage the shared memory (see column 6, lines 44-50), the method comprising the steps of: at the first processor:

- (a) allocating a memory buffer from the shared memory for use in loading a message to be sent to the second processor in response to a specific request from the second processor (see lines 51-63 of column 5);

- (b) loading the message in the memory buffer (see lines 51-63 of column 5).

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Johanson fails to teach sending a message buffer pointer to the second processor that directs the second processor to the message buffer.

Ellsworth teaches in an analogous system, the first processor allocating the shared memory (see lines 16-37 of column 3, note the shared resource disclosed by Ellsworth is shared memory (see lines 7-12 of column 5)). Ellsworth further teaches sending a message buffer pointer (see lines 23-39 of column 6) to the second processor that directs the second processor to the message buffer (see paragraph bridging columns 8 and 9, note the pointer is sent to the second processor via the resource queue).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Johanson with the above teachings of Ellsworth. One of ordinary skill would have been motivated in order to reduce the overhead associated with other methods of sharing memory between two processors as suggested by Ellsworth (see lines 51-67 of column 3).

11. Referring to claim 18, Johanson teaches the first processor sending the starting address of the allocated memory buffer to a

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memory located in the second processor (see lines 18-36 of column 6).

12. Referring to claim 19, Johanson teaches the first processor sends an interrupt to the second processor once it has loaded the starting address of the allocated memory buffer in the memory located in the second processor (see lines 18-36 of column 6).

13. Claims 4-6, 12-14, 16, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Johanson in view of Ellsworth as applied to claims 1, 11, and 15 above, and further in view of McKenney et al. (U.S. Patent No. 6,823,511 hereinafter "McKenney").

14. Referring to method claims 4-6 and apparatus claims 12-14, and apparatus claims 16 and 17, the combination of Johanson and Ellsworth teaches the first processor reads the message from the shared memory after it has been written by the second processor and the first processor releasing the message buffer after the message has been read (see Johanson, see lines 38-48 of column 4).

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The combination of Johanson and Ellsworth fails to teach the second processor passes the message buffer pointer to the first processor and the first processor reading the message from the buffer in response to receiving the message buffer pointer.

McKenney teaches, in an analogous system, returning a pointer from a second processor to a first processor that previously sent the pointer to the second processor for reading a message from the second processor to the first processor (see lines 40-45 of column 11).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Johanson and Ellsworth with the above teachings of McKenney in order to provide proper synchronization between the processors by only allowing one processor at a time to access the shared memory (see lines 6-15 of column 2).

Response to Arguments

15. Applicant's arguments filed 2/13/07 have been fully considered but they are not persuasive. The applicant argues:

1) The cited prior art fails to teach the new limitations of the shared memory including the transmit memories of both processors and the first processor is the master processor (see paragraph bridging pages 7 and 8);

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2) Ellsworth fails to teach a first processor sending a message buffer pointer to the second processor, instead teaches the first processor blindly making portions of memory available.

16. As per arguments 1, the Examiner disagrees. Johanson teaches the shared memory includes the transmit memories for both processors. Figure 1A shows a memory device logically partitioned into three portions. Transmit memories for both processors are at opposite ends of the shared memory. As for the master processor limitation, Johanson does teach the first processor is a master to the second processor, in the sense that *the second processor has to request access to the unallocated portion of memory from the first processor* (emphasis added).

The applicant recognizes this teaching of Johanson (see lines 8-11 of page 8 of applicant's remarks). There is no limitation ⁱⁿ ~~is~~ the claims reciting any limitation concerning write access to various portions of the shared memory. The claim requires that the first master processor manage the shared memory and allocate space to the second processor. At lines 44-50 of column 6, Johanson teaches one possible implementation in which the first processor has access to the dynamic unallocated portion, while the only way the second processor would be allowed to write to

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this unallocated portion is by requesting write access from the first processor (see col. 6, lines 44-50).

17. As per argument 2, the Examiner disagrees. The first processor sends message buffer pointers to a second processor via a resource queue, i.e. the first processor inserts pointers in the resource queue with the intention of having them removed by the second processor (see lines 23-49 of column 7 and paragraph bridging columns 8 and 9).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eron J. Sorrell whose telephone number is 571 272-4160. The examiner can normally be reached on Monday-Friday 8:00AM - 4:30PM.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EJS
March 26, 2007

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March 27, 2007